IN THE CLAIMS

Please cancel claim 15 and add new claims 22-28 without prejudice or disclaimer. The claims are as follows:

1. (Original) A field effect transistor formed in a semiconductor layer which has a strain effect and which is formed in an upper layer of a semiconductor substrate, said field effect transistor comprising:

a source/a drain formed only in said semiconductor layer having the strain effect.

2. (Original) A field effect transistor according to claim 1, wherein said semiconductor layer having the strain effect comprises a silicon layer having a strain effect.

3. (Original) A field effect transistor according to claim 2, further comprising:

silicon epitaxial layers formed on said source/drain; and

refractory metal silicide layers formed on said silicon epitaxial layers.

4. (Original) A field effect transistor according to claim 2, wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

5. (Original) A field effect transistor according to claim 3, wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

6. (Original) A method of fabricating a field effect transistor, comprising the steps of:

forming a semiconductor substrate in such a manner that a semiconductor layer having a strain effect is formed in an upper layer of said semiconductor substrate;

forming a gate electrode on said semiconductor layer having the strain effect through a gate insulating film; and

forming a source/a drain by doping an impurity for forming the source/drain in said semiconductor layer having the strain effect on both sides of said gate electrode.

7. (Original) A method of fabricating a field effect transistor according to claim 6, wherein said semiconductor layer having the strain effect comprises a silicon layer having a strain effect.

8. (Original) A method of fabricating a field effect transistor according to claim 7, further comprising the steps of:

forming, after formation of said source/drain, silicon epitaxial layers on said source/drain; and

forming refractory metal silicide layers on said silicon epitaxial layers.

9. (Original) A semiconductor device comprising:

a p-channel type field effect transistor and an n-channel type field effect transistor both formed in a semiconductor layer which has a strain effect and which is formed in an upper layer of a semiconductor substrate,

wherein a source/a drain of said p-channel type field effect transistor and a source/a drain of said n-channel type field effect transistor are formed only in said semiconductor layer having the strain effect.

10. (Original) A semiconductor device according to claim 9, wherein said semiconductor layer having the strain effect comprises a silicon layer having a strain effect comprises a silicon layer having a strain effect.

11. (Original) A semiconductor device according to claim 10, wherein each of said p-channel type field effect transistor and said n-channel type field effect transistor comprises:

silicon epitaxial layers formed on said source/drain; and

refractory metal silicide layers formed on said silicon epitaxial layers.

12. (Original) A semiconductor device according to claim 10, wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

13. (Original) A semiconductor device according to claim 11, wherein said semiconductor substrate comprises:

a silicon base;

a buffer layer formed on said silicon base, said buffer layer being made from silicon germanium in which the concentration of germanium is changed in the thickness direction;

a relax layer formed on said buffer layer, said relax layer being made from silicon germanium whose stress is relaxed; and

a silicon layer formed on said relax layer, said silicon layer having a strain effect.

14. (Previously Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a semiconductor substrate in such a manner that a silicon layer having a strain effect is formed in an upper layer of said semiconductor substrate, a relax layer is formed below

the silicon layer having the strain effect, and a buffer layer below the relax layer;

forming a gate electrode of a p-channel type field effect transistor and a gate electrode of a-n channel type field effect transistor on said strain effect silicon layer through a gate insulating film;

forming a source and a drain each composed of p-type diffusion layer in only said strain effect silicon layer on both sides of said gate electrode of said p-channel type field effect transistor, the source and drain of the p-type diffusion layers being formed to a depth of less than a depth of the strain effect silicon layer;

forming a source and a drain each composed of n-type diffusion layers in only said strain effect silicon layer on both sides of said gate electrode of said n-channel type field effect transistor, the source and drain of the n-type diffusion layers being formed to a depth of less than a depth of the strain effect silicon layer;

forming a isolation region in between the p-channel type field effect transistor and the n-channel type field effect transistor in said silicon layer having the strain effect; and

wherein the buffer layer is constructed of a P^- type silicon germanium, wherein the relax layer is made from a P^- type silicon germanium whose stress is relaxed.

15. (canceled)

16. (Original) A logic circuit comprising:

a semiconductor device having a p-channel type field effect transistor and an n-channel type field effect transistor;

wherein a semiconductor substrate on which said logic circuit is formed comprises a

semiconductor substrate in which a silicon layer having a strain effect is formed in an upper layer thereof;

a source/a drain of said p-channel type field effect transistor are formed only in said silicon layer having the strain effect; and

a source/a drain of said n-channel type field effect transistor are formed only in said silicon layer having the strain effect.

17. (Original) A semiconductor substrate comprising:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

18. (Original) A field effect transistor according to claim 2, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

19. (Original) A field effect transistor according to claim 3, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

20. (Original) A semiconductor device according to claim 10, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

21. (Original) A semiconductor device according to claim 11, wherein said semiconductor substrate comprises:

a germanium base;

a relax layer formed on said germanium base, said relax layer being composed of a silicon germanium layer whose stress is relaxed; and

a silicon formed on said relax layer, said silicon layer having a strain effect.

22. (Newly-added) A method of fabricating a field effect transistor as set forth in claim 6, wherein the step of forming a semiconductor substrate is further limited in that semiconductor layer is a silicon layer.

23. (Newly–added) A method of fabricating a field effect transistor as set forth in claim 6, wherein the step of forming a gate electrode is further limited in that semiconductor a gate electrode of a p-channel type field effect transistor and a gate electrode of an n-channel type field effect transistor are formed on a silicon layer having the strain effect through a gate insulating film.

24. (Newly-added) A method of fabricating a field effect transistor as set forth in claim 6, wherein the step of forming a source/a drain is further limited in that impurity is an n-type diffusion layer so that said n-type diffusion layers said silicon layer are formed having the strain effect on both sides of said gate electrode.

25. (Newly-added) The method of claim 14, further comprising the steps of:

forming silicon epitaxial layers on the source and on the drain;

forming refractory metal silicide layers on the silicon epitaxial layers.

26. (Newly-added) The method of claim 14, further comprising the step of forming a isolation region in between the p-channel type field effect transistor and the n-channel type field effect transistor in said strain effect silicon layer.

27. (Newly-added) A method of fabricating a semiconductor device, comprising the steps of:

forming a semiconductor substrate by

forming a buffer layer on a silicon base layer, wherein the buffer layer is made of a P^- type silicon germanium,

forming a relax layer on the buffer layer, wherein the relax layer is formed of P^- type silicon germanium which is relaxed, and

forming a silicon strain effect layer on the relax layer;

forming a gate electrode of a p-channel type field effect transistor and a gate electrode of a n-channel type field effect transistor on said strain effect silicon layer through a gate insulating film;

forming a source and a drain each composed of p-type diffusion layers only in said silicon layer having the strain effect on both sides of said gate electrode of said p-channel type field effect transistor, the source and drain of the p-type diffusion layers being formed to a depth of less than a depth of the strain effect silicon layer;

forming a source and a drain each composed of n-type diffusion layers only in said strain effect silicon layer on both sides of said gate electrode of said n-channel type field effect transistor, the source and drain of the n-type diffusion layers being formed to a depth of less than a depth of the strain effect silicon layer; and

forming a isolation region in between the p-channel type field effect transistor and the n-channel type field effect transistor in said strain effect silicon layer.

28. (Original) The method of claim 27, further comprising the steps of:

forming silicon epitaxial layers on the source and on the drain;

forming refractory metal silicide layers on the silicon epitaxial layers.